GaAs MESFET Modeling and Nonlinear CAD

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(*Invited Paper*)

Abstract—**Equivalent circuit modeling techniques are described for both small-signal and large-signal models of GaAs MESFET's. The use of the large-signal model in an interactive program for amplifier analysis is shown. The computed load-pull results and IMD predictions are shown to be in good agreement with measured data at 10 GHz.**

I. Introduction

STATE-OF-THE-ART computer-aided design (CAD) methods for active microwave circuits rely heavily on models of real devices. The equivalent circuit device models must be based upon accurate parameter extraction from experimental data. One purpose of this paper is to clarify the calibration of equivalent circuit models used for GaAs MESFET's. Both small-signal and large-signal models will be discussed.

The second purpose of this paper is to describe an analysis technique used with the large-signal GaAs MESFET model. This technique, called harmonic balance, is allowing the development of new CAD tools useful for the design of microwave integrated circuits (MIC's) and monolithic microwave intergrated circuits (MMIC's).

II. Small-Signal Device Modeling

Previous attempts to construct FET models were based only on S-parameter measurements. But Vaitkus [1] has shown that the errors associated with measuring and de-embedding device scattering parameters leads to significant errors in the equivalent circuit element values for GaAs FET's. Some of these errors can be reduced with improved S-parameter measurement techniques such as the through, short, delay (TSD) approach [2] and the technique of Bianco *et al.* [3], wherein the effects of RF launchers are accurately removed. However, GaAs power FET's are carrier-mounted and therefore are surrounded by more parasitic circuit elements and require additional de-embedding.

Part of the problem is that there are too many variables to create a unique solution based only upon a set of broad-band S-parameter measurements. The situation is even worse for characterization of GaAs dual-gate FET's. Tsironis and Meierer [4] attempt to resolve 28 circuit element values from 3-port S-parameter data. As they discuss, the optimization process is hopeless unless started with accurate estimates of most circuit element values from independent measurements or calculations.

In this paper, an accurate and unique equivalent circuit model is developed by using three different automated measurements of the carrier-mounted FET:

1) The FET mounted in its carrier is measured using a test fixture where the chip is only a connector away from the measurement reference plane where the calibration occurs. A recent improvement in this technique is the use of electrically short 3.5-mm connectors. These connections are SMA compatible, low loss, and resonance free to 34 GHz.

S-parameter measurements with zero drain-to-source voltage ("cold FET" data) are made. These data are used to determine the external parasitics, such as bond wire inductance and carrier stand-off capacitance (these measurements must be made just before the hot, or drain-source biased, S-parameter tests).

2) Hot FET S parameters are measured.

3) The gate (R_g), source (R_s), and drain (R_d) resistances are measured using an automated Fukui approach [5].

With these additional measurements the number of unknown variables is reduced from a total of 16 to 8. This makes it much easier to determine an accurate and unique model that fits the measured data for the FET.

A. Zero-Bias Measurements

As Diamond and Laviron [6] have suggested, the S-parameter measurements for a device with $V_{ds} = 0$ V permit more accurate evaluation of device parasitics because the equivalent circuit is much simpler. Fig. 1 shows the lumped-element equivalent circuit of the carrier-mounted FET for the case of zero biasing. Using S-parameter data for device B1824-20C from 4 to 18 GHz, all circuit element values were optimized for a minimum calculated error function in the program SUPER-COMPACT [7]. For small differences in the error function, the optimum values of R_g, R_s, and R_d vary widely depending upon the optimization method and the starting values. For example, R_s

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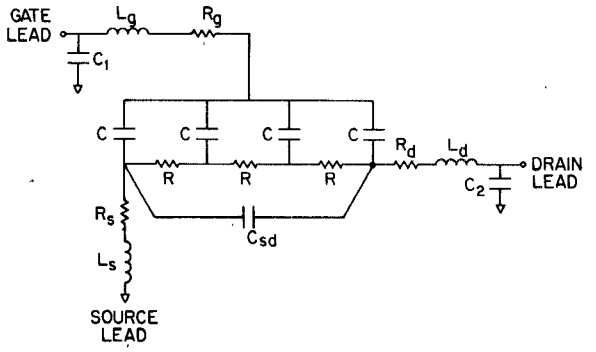

Fig. 1. Equivalent circuit of carrier-mounted FET at zero drain–source bias voltage.

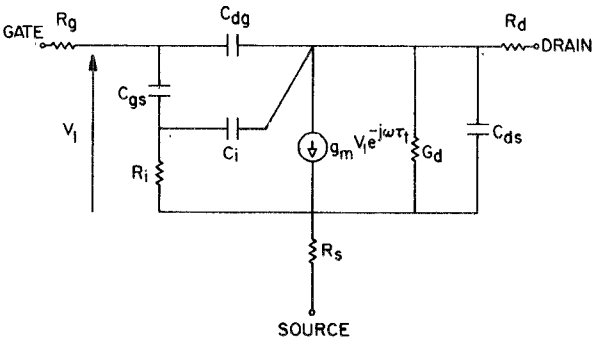

Fig. 2. FET chip equivalent circuit at normal operating bias.

TABLE I
OPTIMIZED CIRCUIT ELEMENT VALUES FOR FET 1824-20C WITH $V_{ds} = 0$ V FOR 4–18 GHz RANGE WITH $R_g = 0.549\ \Omega$, $R_s = 1.048\ \Omega$, $R_d = 1.367\ \Omega$, $C_1 = 0.044$ pF, $C_2 = 0.039$ pF

V_{gs} (V)	R (Ω)	C (pF)	C_{sd} (pF)	L_g (nH)	L_d (nH)	L_s (pH)
0.0	0.3354	0.2289	0.1730	0.3115	0.2514	10.71
−1.0	0.5143	0.1814	0.1726	0.3134	0.2507	10.73
−2.0	0.7593	0.1620	0.1725	0.3158	0.2516	10.48

varied between 0 and 0.7 Ω, R_g varied between 0.9 and 1.53 Ω, and R_d varied between 0.5 and 1.3 Ω. Clearly the value of $R_s = 0$ Ω is nonphysical as one expects R_s to be very nearly the same as R_d due to the construction of the device. It is interesting to note that the values of L_s, L_d, L_g, R, and C did not vary more than ±1 percent for these cases, even with widely varying resistance values.

To resolve this accuracy problem, we use resistance values determined from dc measurements of the type described by Fukui. These resistance values give the best approximation available. Using these values, Table I shows the values of the other circuit elements for three values of V_{gs} for $V_{ds} = 0$. The values of R and C vary with gate bias, as expected, and the inductive circuit elements vary less than 2 percent. The calculated S parameters for this optimized model are extremely close to the measured data. The values R and C are not used for subsequent modeling at full bias but may be used for diagnostic information about the gate and the conduction channel.

B. FET Modeling at Full-Bias Voltage

Subsequent S-parameter measurements at full operating bias can then be used to resolve the FET chip into an RF equivalent circuit of the type shown in Fig. 2. Using this procedure, the final FET model has only eight unknown elements (in the FET chip) out of a possible 16 (in the carrier-mounted FET). The accuracy of this procedure has been discussed earlier [8].

The circuit model of Fig. 2 has several important advantages over other configurations. The internal feedback capacitor C_i physically results from drain-to-channel feedback and causes the reverse transfer conductance (i.e., drain-to-gate) to have positive sign and square-law frequency dependence. This behavior is also observed in our two-dimensional simulation [8] as well as in laboratory measurements. The current source is controlled by the total voltage across the (gate) capacitor C_{sg} and the (channel) resistor R_i rather than by the voltage across C_{sg} alone. This forces the time-delay factor τ_t to account for all delay effects under the gate and permits the value of R_i to be based only upon input loss. By comparing the Y parameters of the chip's equivalent circuit model with those of an accurate two-dimensional FET model [9], we find the equivalent circuit model to be accurate to about 50 GHz.

As discussed earlier, the resistance values R_g, R_s, and R_d are obtained from Fukui measurements, and inductance values are obtained from the $V_{ds} = 0$ measurements. The remaining values of the FET circuit elements are optimized for best agreement with the experimental data. It is interesting to compare the Y parameters of the FET chip model with experimental data. The experimental Y parameters are obtained by de-embedding the device from the carrier at each RF frequency. In all cases, the inductances used are fixed and equal to the values obtained from zero drain–source bias measurements.

Fig. 3 shows the comparison of the final model and the data for Y_{11} for device B1824-20C. The agreement becomes progressively worse as frequency is increased and the functional behavior of the experimental data with frequency is nonphysical above 18 GHz. The parameters Y_{21} and Y_{22} show similar behavior. This departure from the theoretically expected behavior means that only data up to 18 GHz are accurate. Notice that the actual error between the data and final model is not large. The horizontal scale has been expanded for clarity in Fig. 3. The model was optimized for the frequency range 6–18 GHz. Optimization over a larger (or smaller) range does not change the functional form of the Y parameters.

Fig. 4 shows the Smith chart values of S_{11} and S_{22} computed using the FET model (including the carrier) and the measured data. The errors are clearly more apparent in Fig. 3 than in Fig. 4. Figs. 5 and 6 show S_{12} and S_{21}, respectively. Errors are small. FET's measured and modeled a second time (after disassembly from the test fixture) show only small changes in the values of equivalent circuit elements.

A second example will illustrate the uncertainty of the element values when determined from S-parameter data.

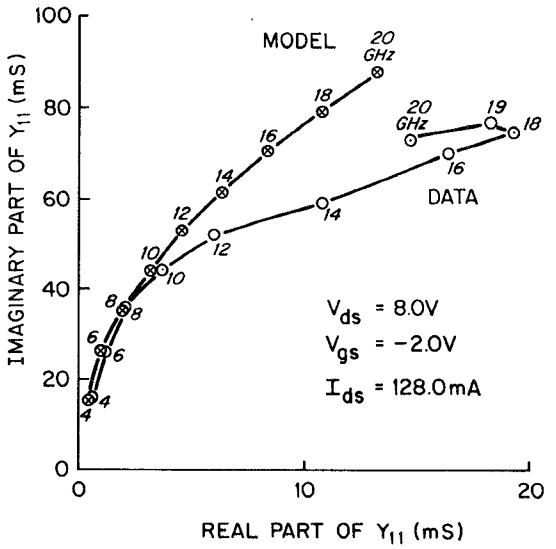

Fig. 3. Admittance parameter Y_{11} as function of frequency for the FET chip and for the de-embedded data.

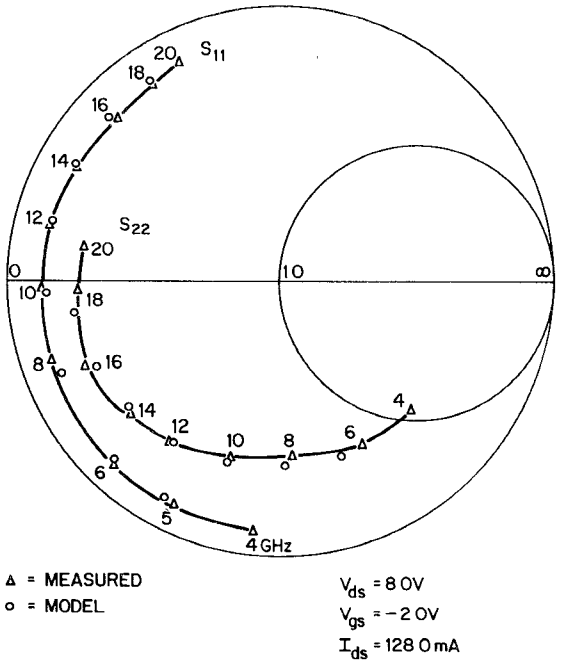

Fig. 4. Smith chart display of measured data and model for S_{11} and S_{22} for the carrier-mounted FET.

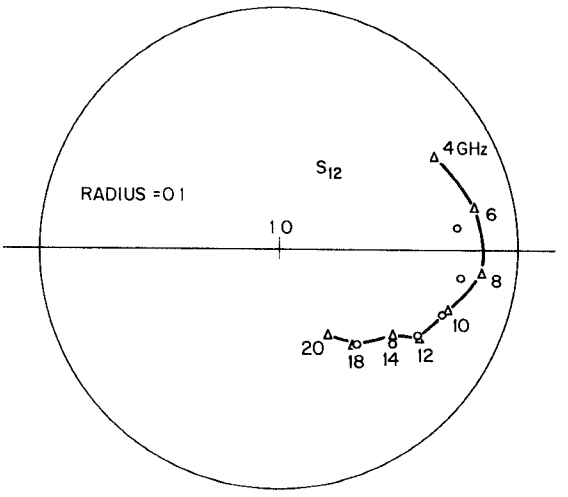

Fig. 5. Smith chart display of S_{12}.

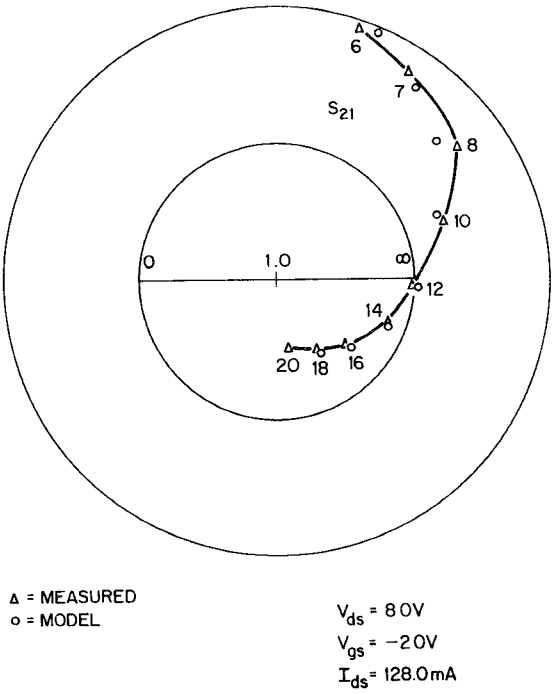

Fig. 6. Smith chart display of S_{21}

A FET with mounting parasitics has 18 electrical elements (or parameters). S-parameter data were taken in 1 GHz steps from 6 GHz to 18 GHz and the program SUPER-COMPACT was used to optimize the element values for agreement with the data, starting with several different sets of initial values. Each case converged but had slightly different optimum values of each circuit element. The variation in each element value is a measure of the uncertainty in the element value (due to the optimization algorithm).

Tables II and III present the results of this study in comparison with the procedure recommended here. Table II shows that the uncertainty in the source inductance is over 25 percent, which is quite significant. Table III shows that the uncertainty in the FET's element values is significantly larger when determined only from hot S-parameter data.

There is also uncertainty introduced due to measurement inaccuracies. That is, a second measurement would produce slightly different data. This is an additional reason for using data in addition to the usual (hot) S-parameter data for the determination of FET element values. The uncertainty produced in the procedure recommended here is much less dependent upon the algorithm used for optimization. Many of these conclusions were independently verified by Vaitkus and the reader is referred to his study for further information.

TABLE II
PERCENTAGE CHANGE IN PARASITIC INDUCTANCES FOR SEVERAL TRIALS WITH OPTIMIZATION PROGRAM (S-PARAMETERS MEASURED 6 GHz–18 GHz, 1 GHz STEPS)

	Cold FET	18-Parameter Model
	(%)	(%)
L_g	1.4	6.6
L_d	0.4	6.2
L_s	4.6	25.7

TABLE III
PERCENTAGE CHANGE IN THE ELEMENT VALUES FOR SEVERAL TRIALS WITH OPTIMIZATION PROGRAM (S-PARAMETERS MEASURED 6–18 GHz, 1 GHz STEPS)

	7-Parameter Model	18-Parameter Model
	(%)	(%)
C_{gs}	1.9	7.4
R_i	27.0	52.4
C_{dg}	2.0	7.9
G_m	2.6	10.0
τ	3.3	4.6
R_{ds}	1.8	6.6
C_{ds}	0.7	3.8
G_m/C_{gs}	1.4	2.4

III. TIME-DOMAIN FET MODELS AND SIMULATION TECHNIQUES

Nonlinear FET operation produces nonsinusoidal current and voltage waveforms at both the input and the output ports. Since the nonlinearities of the FET depend on the instantaneous voltages and currents, analysis of the FET is most accurately accomplished in the time domain. Analysis in the frequency domain by techniques such as the Volterra series is limited to weak nonlinearities because of the slow convergence of the series for strong nonlinearity.

The general-purpose nonlinear circuit analysis programs that exist were designed primarily for transient (time domain) analysis of silicon integrated circuits [10], [11]. By adding new models for GaAs devices, Curtice [12] and Sussman-Fort *et al.* [13] show that these programs can be used for studying GaAs integrated circuits. However, a more sophisticated model is required to study GaAs power FETs operated at high dc-to-RF conversion efficiency. Such a model must contain an accurate description of all the important device nonlinearities and also efficiently analyze the external microwave circuit interaction over many RF cycles. The circuit reactances lead to time constants that are large relative to the RF period. Time-domain analysis is then very inefficient.

An additional problem encountered often with time-domain simulation programs, such as SPICE [10], is the lack of convergence for certain input data conditions. Sometimes the program appears to converge but, in fact, the results are nonphysical. The same problem has been observed, R-CAP, RCA's proprietary circuit simulation program.

Although it may be possible to eliminate the numerical instability we found in R-CAP, both R-CAP and SPICE require lengthy execution times to reach steady state. Ironically, it is the external linear circuit elements that cause this effect. In addition, neither the recent model of Golio *et al.* [14] nor the model of Curtice [12] is sufficiently detailed for amplifier design. For instance, neither model includes drain–gate avalanche breakdown currents. If we start with a very detailed two-dimensional (2-D) GaAs FET model, such as that described by Curtice and Yun [15], it is possible to add external circuits and develop time-domain solutions, as with R-CAP. The problem here is that the FET model is already quite CPU intensive. Adding external circuits increases the problem. Even with simple external circuits, the 2-D model must run overnight on a VAX 11/780 to reach a steady-state solution. This clearly is not useful as an interactive design tool.

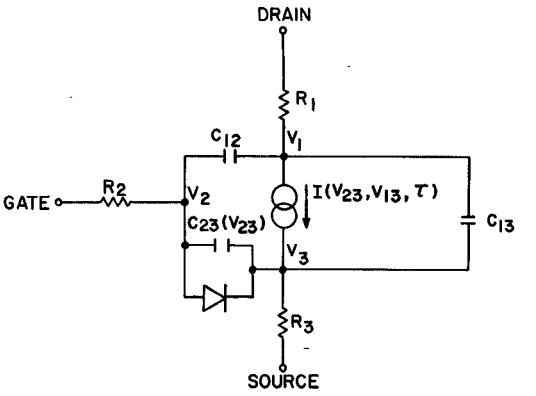

Fig. 7. Circuit model no. 1 of the GaAs MESFET for use with a circuit analysis program.

IV. GaAs MESFET MODEL No. 1

The JFET model in SPICE [10] is widely used for GaAs circuit simulation studies. However, this model has several deficiencies when applied for GaAs MESFET's. As will be shown, this model is quite in error with regard to drain current–voltage relationships below current saturation. Furthermore, electron transit-time effects under the gate are omitted.

Fig. 7 is the large-signal model [12] developed in 1980 for the GaAs MESFET used in digital IC's. It consists primarily of a voltage-controlled current source $I(V_{23}, V_{13}, \tau)$, three interelectrode capacitors, and a clamping diode between gate and source. Resistors R_1, R_2, and R_3 represent resistance of the contact regions. The nonlinear elements are $I(V_{23}, V_{13}, \tau)$, $C_{12}(V_{12})$, and $C_{23}(V_{23})$. The important aspects of the evaluation of current will now be described.

The drain current relationship to drain–source voltage and gate–source voltage is usually known either from experimental measurements of test devices or from detailed device calculations. The MESFET model must use analytical expressions to approximate this relationship. Often several parameters are required and must be determined by curve-fitting techniques. Analytical analysis of the symmetrical JFET model (see Sze [16]) results in a (gate) voltage-controlled drain current source (in the cur-

rent saturation region) of the form

$$I_{ds} = I_p \left[1 + \frac{V_{gs} + V_{bi}}{V_p} \right]^N \tag{1}$$

where I_p is the "pinch-off current" as defined by Sze and more commonly called saturation current; V_p is the pinch-off voltage, which is $qN_0a^2/(2\epsilon)$ for uniform doping; V_{bi} is the built-in voltage at the gate (a negative voltage); V_{gs} is the gate–source voltage; a is the active layer thickness; and N_0 is the donor value. N is found to vary between 2.0 and 2.25, depending upon the charge distribution assumed. It can be shown that the square-law assumption is quite good for real devices [16].

Equation (1) can be put in a standard form as

$$I_{ds} = \beta_1 (V_{gs} + V_{T0})^2 \tag{2}$$

where V_{T0} is the threshold voltage measured from gate to source, $V_{T0} = V_p + V_{bi}$, and $\beta_1 = I_p/V_p^2$.

Equation (2) is the form in the current saturation region used in the general circuit analysis program SPICE. β_1 and V_{T0} are determined by plotting I_{ds} versus V_{gs}. If actual experimental values of I_{ds} are used, then a current source without source resistance is being described. To develop the model of Fig. 7, the raw data must first be processed to remove the effects of R_1 and R_3. This can easily be accomplished once the values of R_1 and R_3 are determined either by measurements [5] or by calculations. Since the voltage drop across R_3 is typically not negligible, the presence of R_3 usually has a major effect.

The current saturation in GaAs MESFET's occurs at lower voltages than in silicon devices because of the much larger low field mobility. This results in a much stronger current saturation effect. Van Tuyl and Liechti [17] point out that the hyperbolic tangent function provides a good analytical expression for current saturation in GaAs. In addition, one also wants to be able to describe drain–source conductance effects. This is not adequately described by adding a shunt resistor across $I(V_{23}, V_{13}, \tau)$ because current pinch-off is lost. The expression used in SPICE seems to fit experimental devices quite well in the region of current saturation. The expressions used in SPICE are derived from the FET model of Shichman and Hodges [18].

The use of the hyperbolic tangent function greatly improves the usefulness of the equation below saturation. The following analytical function is proposed for description of the current source in GaAs MESFET's:

$$I(V_{23}, V_{13}) = \begin{cases} \beta_1 (V_{23} + V_{T0})^2 \cdot (1 + \lambda V_{13}) \tanh(\alpha V_{13}) & V_{23} + V_{T0} \geq 0 \\ 0 & V_{23} + V_{T0} < 0 \end{cases} \tag{3}$$

where α and λ are constants. Notice that there are four parameters to be evaluated in this expression.

Equation (3) was used to approximate a set of measured drain current–voltage relationships presented by Van Tuyl and Liechti. The experimental data can be matched quite accurately. Fig. 8 shows the characteristics calculated from (3). For comparison purposes, the JFET model of SPICE was also used and these computations are shown in Fig. 8 as dashed lines. Notice that although the gate control is accurately given by both models in the region of current saturation, the SPICE calculations are quite in error below current saturation due to the lack of a parameter to adjust the saturation point. This is a major deficiency of the SPICE model and leads to significant error in computations of switching characteristics.

During transient operation, a change in gate voltage does not cause an instantaneous change in drain–source conduction current. This results because in order for conduction current to change, the electron depletion width under the gate must be changed and this occurs by charge transport at a velocity of approximately 1×10^7 cm/s. Thus, it takes of the order of 10 ps for a change in current after the gate voltage is changed in a 1 μm gate length MESFET. (Notice that in the physical device, this charge change is part of the gate capacitance change, whereas in the model we have separated the capacitance and current effects.) The most important result of this effect is a time delay produced between gate–source voltage and drain current. Therefore, the current source, (3),

$$I[V_{23}(t), V_{13}]$$

should be altered to

$$I[V_{23}(t - \tau), V_{13}]$$

where τ is equal to the transit time under the gate.

The time delay effect is not easily added to most circuit analysis programs. We have found a technique that accurately approximates the effect but is simple to calculate. The current source is assumed to be of the form

$$I(v) - \tau \frac{dI(v)}{dt} \tag{4}$$

where the derivative is evaluated as

$$\frac{dI(v)}{dt} = \left[\frac{dI(v)}{dV} \right]_{V_{13}} \cdot \frac{dV_{23}}{dt}. \tag{5}$$

The second term in (4) is a correction term, which may be thought of as the first term of the expansion of $I(t - \tau)$ in time. If τ is not included, an important source of delay in any MESFET circuit is omitted.

The present model included transit time effects in driving and source-follower transistors, but not in transistors used for active loads since $dV_{23}/dt = 0$. A MESFET logic circuit would use all three types of operation (Van Tuyl and Liechti [17]).

The model shown in Fig. 7 may be used with a circuit simulation program to study complex integrated circuits. The circuit simulation program used here is R-CAP [11]. It is similar to SPICE in many respects but has the advantage that a user-defined device model can be included without

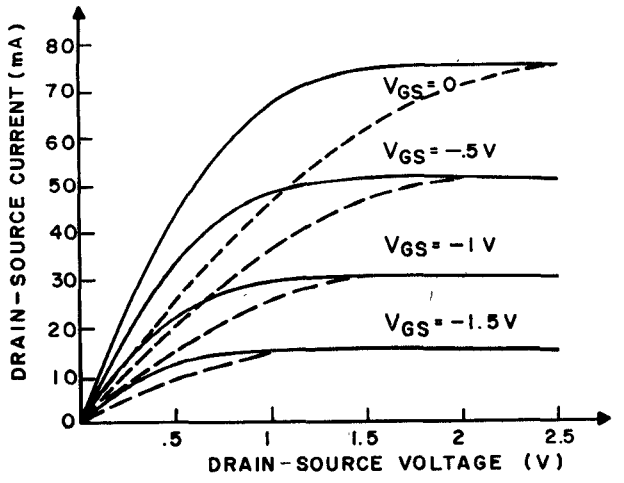

Fig. 8. Best-fit approximation to experimental MESFET I–V characteristics using the current source described by eq. (3) (solid lines) and by the JFET model of SPICE 2 (dashed lines).

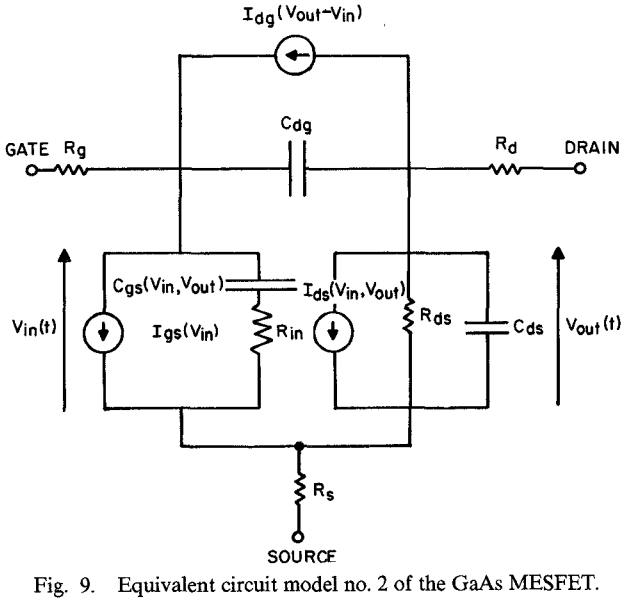

Fig. 9. Equivalent circuit model no. 2 of the GaAs MESFET.

difficulty. The model for GaAs MESFET was added to R-CAP as a subroutine and used in many simulations of IC designs being developed.

V. GaAs MESFET Model No. 2

Fig. 9 shows the equivalent circuit model assumed. This model is noticeably different than presented earlier for accurate small-signal modeling of GaAs MESFET's. The drain-channel capacitor is omitted to simplify node current equations. This produces some loss of accuracy. In addition, two new current sources are used. The drain–gate voltage-controlled current source represents the drain–gate avalanche current that can occur at large-signal operation. The gate–source voltage-controlled current source represents gate current that occurs when the gate–source junction is forward biased. The third current source, $I_{ds}(V_{in}, V_{out})$, is the large-signal form of the usual small-signal transconductance.

Model no. 1 assumes a square-law relationship between the (saturation) current and the gate–source voltage. Although this form has advantages, it is more accurate to use a cubic approximation:

$$I_{ds} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right) \cdot \tanh\left(\gamma V_{\text{out}}(t)\right) \quad (6)$$

where V_1 is the input voltage. The coefficients (A_i) can be evaluated from data in the saturation region at the same time the data are measured.

The following method is used to include the phenomenon of pinch-off voltage increase with drain–source voltage. We assume

$$V_1 = V_{\text{in}}(t-\tau) \cdot \left[1 + \beta_2 \left(V_{ds0} - V_{\text{out}}(t)\right)\right] \quad (7)$$

where β_2 = coefficient for pinch-off change, V_{ds0} = output voltage at which A_0, A_1, A_2, A_3 were evaluated, and τ = internal time delay of FET.

Measured RF data show that τ is a direct function of drain–source voltage, or

$$\tau = A_5 \cdot V_{\text{out}}(t).$$

The drain currents cannot be pinched off at large drain–source voltages due to the gate current produced by avalanche breakdown. This is an important phenomenon, which limits both RF current and power output. In this model, the drain–gate avalanche current is taken to be

$$I_{dg} = \begin{cases} \dfrac{V_{dg}(t) - V_B}{R_1} & V_{dg} > V_B \\ 0 & V_{dg} < V_B \end{cases} \quad (8)$$

where $V_B = V_{B0} + R_2 \cdot I_{ds}$, R_1 is the approximate breakdown resistance, and R_2 is the resistance relating breakdown voltage to channel currents.

The forward-biased gate current is taken to be

$$I_{gs} = \begin{cases} \dfrac{V_{\text{in}}(t) - V_{bi}}{R_F} & V_{\text{in}}(t) \geq V_{bi} \\ 0 & V_{\text{in}}(t) < V_{bi} \end{cases} \quad (9)$$

where V_{bi} is the built-in voltage, and R_f is the effective value of forward bias resistance.

Table IV summarizes the characterization tests required for the FET. The values of R_g, R_d, and R_s are obtained from the automated Fukui measurements. The values of C_{dg}, C_{gs}, R_{ds}, and C_{ds} at the bias point are obtained from the small-signal model using the technique described earlier. Although both C_{gs} and C_{dg} are nonlinear functions of voltage, computation including these characteristics produces only small effects upon the RF power saturation characteristics.

In summary, the equivalent circuit model has been constructed with the circuit shown in Fig. 9. The principal nonlinearities are the voltage-controlled current sources. These must be characterized for each device. It was found to be important to include the bias dependence of pinch-off voltage in the drain-current source.

TABLE IV
FET CIRCUIT MODEL CHARACTERIZATION TESTS

- Fundamental Device Parameter Determination
  (dc $I-V$ and Fukui method)
  $R_s R_d, R_g$
  $I_{ds}(V_{gs}, V_{ds})$
  $I_{gs}(V_{gs})$
- Linear Model and Parasitic Parameter Determination
  (Wide-band S-parameter network analysis)
  Cold FET ($V_{ds} = 0$)
  Hot FET ($V_{ds} > 0$)
- Pulsed Avalanche Measurements
  $I_{dg}(V_{gs}, V_{ds})$

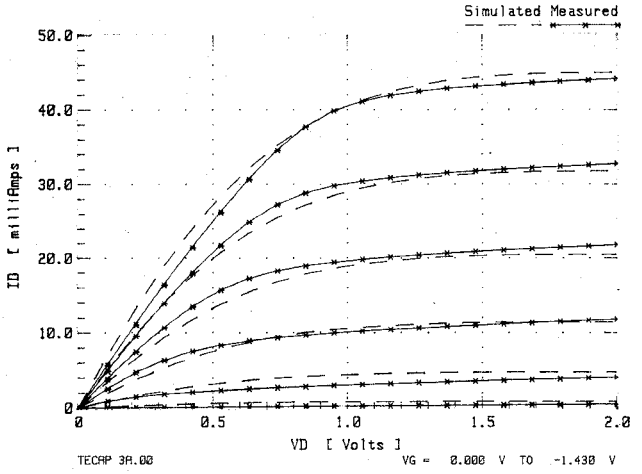

Fig. 10. Experimental data and best match for model no. 1 with maximum $V_D = 2.0$ V (BETA1 = 0.02248, VTO = −1.638, $\alpha = 1.489$, $\lambda = -0.02866$).

VI. COMPARISON OF MODEL NO. 1 AND NO. 2

The program TECAP from Hewlett Packard was used for comparison of the two models. TECAP is a very versatile program for FET measurement, parameter extraction, and optimization. Hewlett Packard defines parameter extraction as the process by which the initial estimates of device parameters are obtained. Optimization is then defined as the process by which the parameters are optimized for best agreement with the data. The modeling community, in general, defines parameter extraction as the complete process by which optimized parameters are obtained.

Although both models were used to fit experimental data, model no. 2 always produced the least error. The parameter extraction process was not found to be necessary and optimization was successful for any starting values if certain precautions were taken.

For best results with either model it is necessary to set the "true" flag for optimizing the absolute error. For cases with the flag equal to "false," good agreement with the data (small RMS error) is obtained only if the initial guesses for parameters are "good" guesses. With a true flag, good agreement was obtained for all initial guesses, including the default values in TECAP.

In general, model no. 1 works best for low-voltage devices. The error becomes too large at larger drain–source voltages. This means that model no. 1 is suitable for GaAs digital IC's that normally operate with low drain–source voltage.

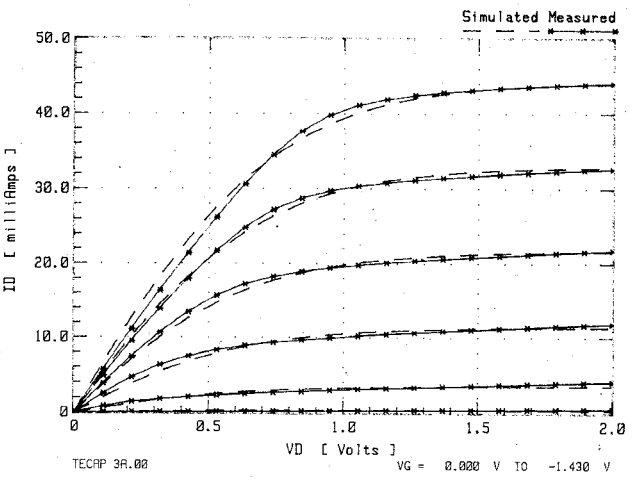

Fig. 11. Experimental data and best match for model no. 2 with maximum $V_D = 2.0$ V (BETA2 = 2.E-22, $A0 = 0.05143$, $A1 = 0.03745$, $A2 = -0.02274$, $A3 = -0.01675$, $\gamma = 1.613$, VDSO = 4.0).

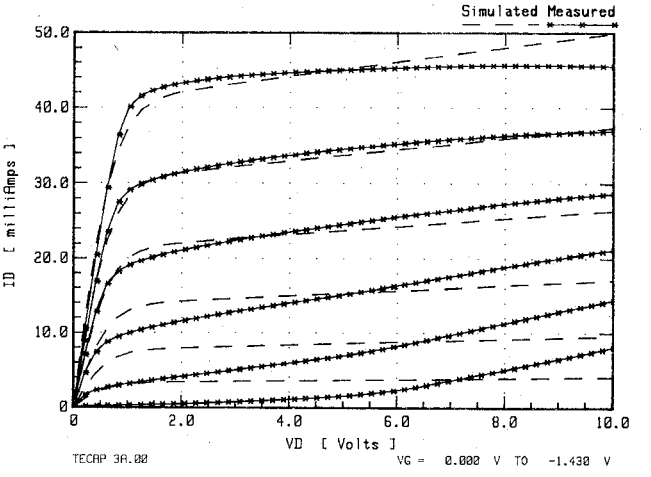

Fig. 12. Experimental data and best match for model no. 1 for maximum $V_D = 10$ V (BETA1 = 0.01266, VTO = −1.946, $\alpha = 1.675$, $\lambda = 0.02983$).

Fig. 10 shows the comparison of the experimental data (crosses) and the device simulation (dash lines) from optimized parameters for model no. 1. Fig. 11 shows the same comparison for model no. 2. The RMS errors in Figs. 10 and 11 are 4.61 percent and 2.49 percent, respectively. For the low drain–source voltage range, either model is satisfactory.

Figs. 12 and 13 show the same results for 10 V maximum drain–source voltage. Table V compares the RMS errors for these cases. This table shows that the error increases with an increase in drain–source voltage range for model no. 1 but it decreases for model no. 2. Indeed, it is extremely impressive that model no. 2 may be made to have such small error for the large range of operating conditions in Fig. 13.

The results for the two models for larger negative gate voltage values are shown in Figs. 14 and 15. Fig. 15, model no. 2, shows a problem at low drain–source voltage due to

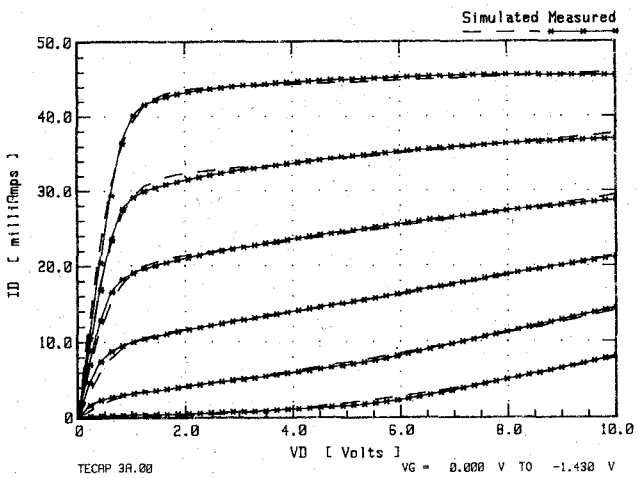

Fig. 13. Experimental data and best match for model no. 2 for maximum $V_D = 10$ V (BETA2 = 0.04062, $A0 = 0.05185$, $A1 = 0.04036$, $A2 = -0.009478$, $A3 = -0.009058$, $\gamma = 1.608$, VDSO = 4.0).

TABLE V
COMPARISON OF ERROR BETWEEN MODEL NO. 1 AND THE EXPERIMENTAL DATA AND MODEL NO. 2 AND THE EXPERIMENTAL DATA

Drain–Source Voltage (V)	RMS Error Model No. 1 (%)	RMS Error Model No. 2 (%)
2	4.61	2.49
6	4.92	1.84
10	7.83	1.47

large negative gate–source voltages. This effect is nonphysical and relates to the β_2 coefficient. β_2 describes the effect of pinch-off voltage changes with drain–source voltage.

It can be seen from Fig. 15 that during optimization the gate voltage range *must* be restricted to values below pinch-off. If this is not done, the effect of nonphysical regions of the model interferes with the optimization process.

VII. N-FET, The New Nonlinear Simulation Program

Camacho-Penalosa [19], Petersen *et al.* [20], Gilmore and Rosenbaum [21], and Materka and Kacprzak [22] all have utilized an analysis technique known as harmonic balance to find steady-state solutions for GaAs FET amplifiers under large-signal operation. We have extended the work of Peterson *et al.* using a more detailed FET model and have developed a useful design tool for the microwave engineer [23].

The program N-FET provides a computer-aided means to develop an output circuit design that optimizes the amplifier performance (i.e., efficiency, bandwidth, etc.). This is made possible by accurate prediction of large-signal load-pull characteristics. The program N-FET consists of a time-domain analysis of the GaAs FET model no. 2 coupled with a frequency-domain analysis of the input- and

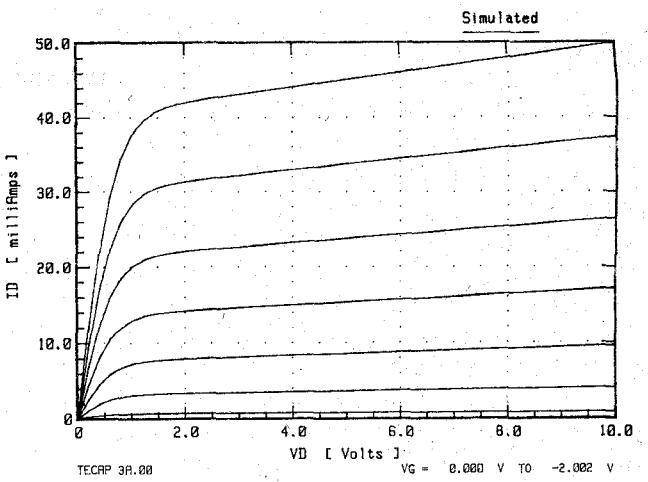

Fig. 14. Simulated characteristics for model no. 1 with maximum $V_g = -2$ V for device parameters the same as Fig. 12.

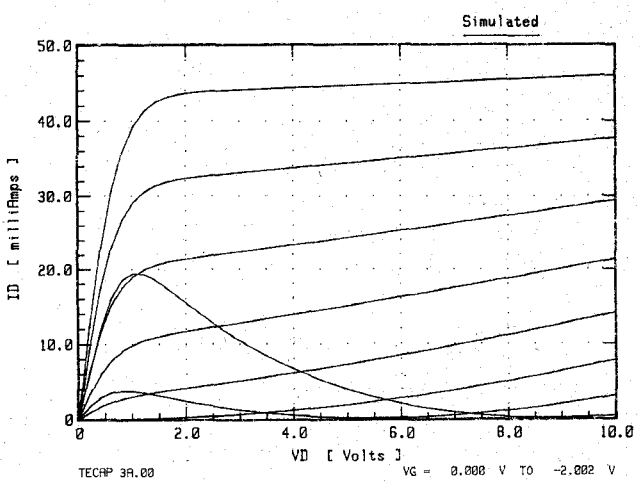

Fig. 15. Simulated characteristics for model no. 2 with maximum $V_g = -2$ V for device parameters the same as Fig. 13.

output-matching circuits. The nonlinear FET elements must be analyzed in the time domain to preserve their physical nature. The linear circuit's response to the FET current excitation can be analyzed in the frequency domain by standard techniques. Transformation between time and frequency domains is accomplished by use of a discrete Fourier transform. A valid physical solution is obtained when the voltage waveform at the input (or output) of the FET produces a current waveform into the device that is the negative of that into the RF circuit to within some small error. The program uses Newton's method of successive approximation to minimize the error between FET currents and external RF circuit currents. Table IV summarizes the characterization tests required for the FET. Pulsed, dc, and RF data are all necessary for accurate characterization.

The amplifier simulation can be performed with voltage waveforms containing fundamental and second-harmonic frequencies or fundamental and second- and third-harmonic frequencies. All FET current harmonics are included. Third-harmonic voltages are used only when accu-

rate circuit impedance data are available at third-harmonic frequency.

N-FET is an interactive program for amplifier analysis and design. It is necessary to create an input data file for N-FET. This file should contain all the device coefficients described earlier and several others. It is necessary to specify the fundamental operating frequency, operating voltage biasing, number of voltage harmonics that need to be included, number of subdivisions of the RF cycle to use in analysis, and the harmonic impedances present at the input and output. The harmonic impedances can be evaluated from measured data or from estimations. These impedances are often difficult to evaluate accurately. An algorithm is used for calculating the load impedance contours of constant power while the input-matching circuit and the drive power are held constant. This feature simulates the experimental load-pull technique [24]. The algorithm is based on the fact that contours of constant power are closed curves on a Smith chart and that a contour of higher power will be enclosed within a contour of lower power.

Load-pull contours are developed as follows: The user specifies the RF drive power. The load for maximum output power is found by the program. Then the load is changed by the user to produce less output power (e.g., -1 dB) and a load contour for constant power is generated.

VIII. Experimental Comparisons

Data presented previously [23] show N-FET to predict load contours in good agreement with measurements for a 600-μm-periphery device. However, more gain is predicted than measured. The discrepancy is thought to be due to tuner loss. A 1200-μm-periphery GaAs MESFET (device "Y") was recently tested with the RCA Programmable Microwave Tuner (PMT) System. The PMT system is a computer-controlled system capable of testing experimental characterization with regard to load impedance for peak output power and load connectors. The final FET load impedance data must be transformed from the standard reference plane of the PMT system to the device's reference plane. This transformation is done automatically by PMT computer system given the reference plane offset data for the APC-7 to SMA transition. The latter data are provided from measurements using an HP8510 network analyzer. The error present in this measurement becomes a very serious problem at higher microwave frequencies.

A double-stub tuner is used to match the input of the FET for maximum power transfer. The tuner loss was evaluated from measurements taken on the HP8510 network analyzer. All components, such as the bias tees, directional coupler, and the pads, were also measured on the HP8510 to accurately determine their insertion losses. The accuracy for any individual measurement was ± 0.1 dB. The resulting uncertainty in the FET's gain is, however, much larger than this because component parts were measured separately and, in addition, the uncertainty in the tuner loss measurement is larger than ± 0.1 dB. We estimate the FET's gain measurement uncertainty to be about ± 0.5 dB.

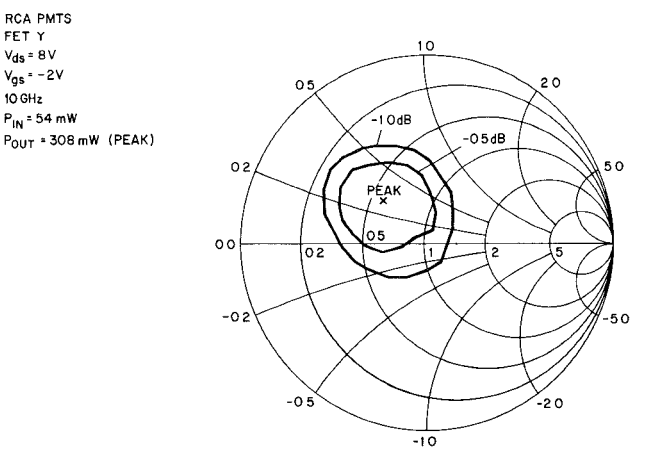

Fig. 16. Smith chart plot of the PMT load-pull data for FET Y operated as a 10 GHz.

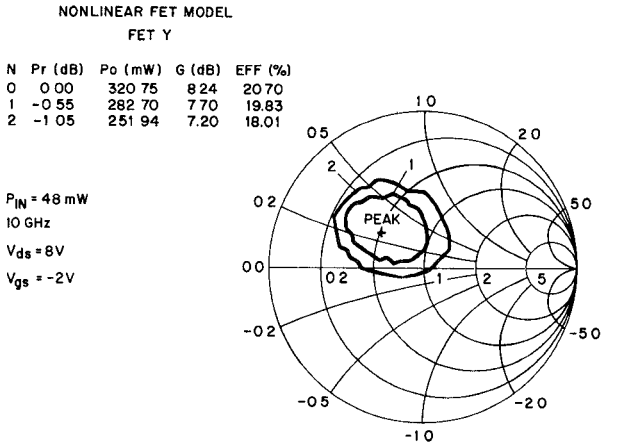

Fig. 17. Smith chart plot of the load-pull characteristics of FET Y as predicted by N-FET, for the same operating conditions as in Fig. 16.

Figs. 16 and 17 show the PMT data and the N-FET results, respectively, for a case of high driver power. The load-pull contours are in excellent agreement. Gain values differ by about 0.7 dB. This is within measurement error. Therefore N-FET quite accurately simulates large-signal behavior.

Device Y was also used for evaluation of the harmonic balance IMD program. These tests were made with two equal input signals. This test is called a "two-tone" test. Figs. 18 and 19 show the PMT data and the N-FET load-pull results, respectively, for the single-tone tests of FET Y with an RF input power of 9.5 mW. Again, the agreement is excellent for the constant power contours. The dashed lines in the figures are the IMD ratios measured from the two-tone tests of the same device. For these data each input signal is 9.5 mW. The IMD values agree best for the load condition of the larger values of IMD. The analysis predicts about 5 dB less IMD for the load conditions producing measured values of -20 to -25 dBc IMD. Overall, the agreement is good. At the load condition for peak power, the analysis predicts -31.2 dBc whereas -26.5 dBc is measured. Fig. 20 shows the varia-

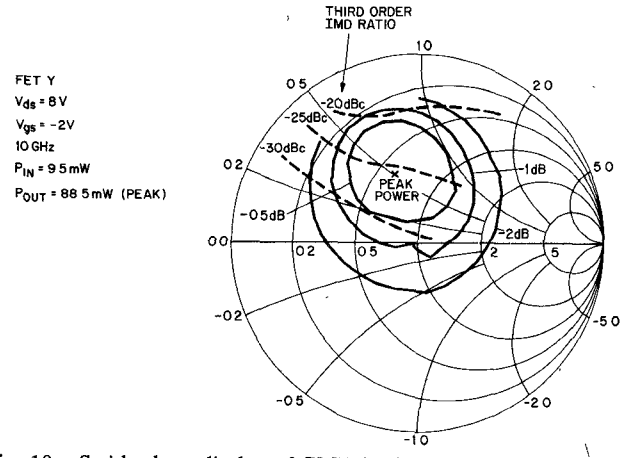

Fig. 18. Smith chart display of PMT load-pull data (solid lines) for FET Y at low RF input power. The dashed lines are the contours of constant third-order IMD measured using two input signals in the PMT system.

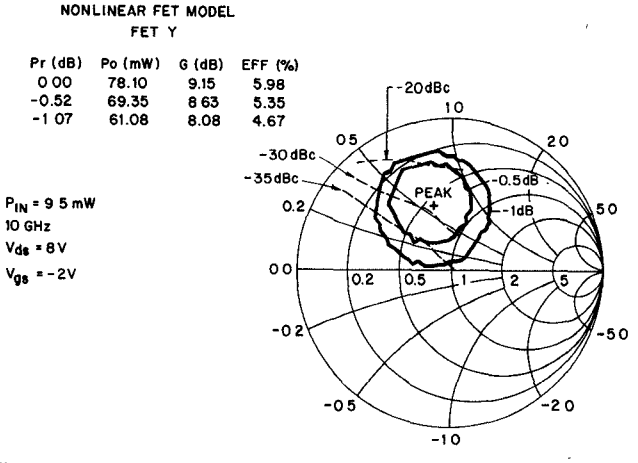

Fig. 19. Smith chart display of the load-pull characteristics (solid lines) and constant IMD contours (dashed lines) for FET Y as predicted by N-FET, for the same operating conditions as in Fig. 18.

tion of two-tone IMD with RF input power for both the calculated IMD and the measured data. Reasonable agreement is present.

The increase in the IMD ratio as the load reflection coefficient is moved toward the outer edge of the Smith chart in Fig. 19 is directly traced to an increase in the drain–source RF voltage amplitude. Likewise, the reduction in IMD ratio as the load reflection coefficient is moved toward the center of the Smith chart is due to a reduction in drain–source RF voltage amplitude. The smaller RF voltage amplitude results in less nonlinear distortion due to the drain–source current–voltage characteristics. Therefore, to trade off output RF power for improved IMD ratio, one should design the load impedance for reduced RF voltage amplitude.

IX. Conclusions

A procedure has been developed for producing small-signal equivalent circuit models for carrier-mounted GaAs FET's for both device design and diagnostic purposes. A prominent feature of this procedure is the reduction of the number of unknown element values to be determined by

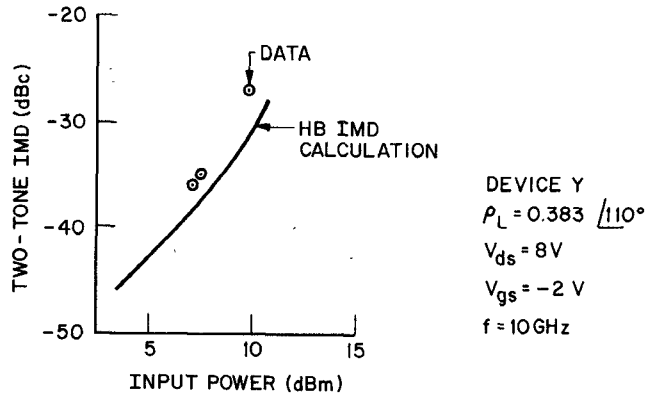

Fig. 20. IMD data (points) and N-FET predictions as a function of RF input power for FET Y when tuned for peak power at low RF drive (see Fig. 18).

S-parameter data, by the use of dc measurements as well as zero-bias measurements. The zero-bias data are used to evaluate the circuit inductances and are taken just before the full-bias data.

The uncertainty in the equivalent circuit element values has been shown to be much less than that produced by the usual method of parameter extraction from *S*-parameter data. Each element value is then more closely related to a physical effect in the FET.

We have also developed a GaAs FET model suitable for efficient simulation of large-signal amplifier operation. The model can be used in an amplifier simulation to develop optimized output network designs for high-power GaAs FET amplifiers. The program's efficiency results from the use of the harmonic balance technique wherein the nonlinear FET is analyzed in the time domain and the linear circuit is analyzed in the frequency domain. The principal nonlinearities of the FET model are voltage-controlled current sources.

The nonlinear FET model was coupled to a program to generate the load required for constant output power contours on a Smith chart. Excellent agreement was obtained with the measured load-pull characteristics and IMD at 10 GHz.

Acknowledgment

The small-signal modeling effort was accomplished with the help of Dr. R. L. Camisa of David Sarnoff Research Center, Princeton, NJ. N-FET was converted to an interactive program by Prof. M. Ettenberg, Professor Emeritus of City College of New York and Consultant to David Sarnoff Research Laboratories. Thanks also to Dr. J. Schepps for help in the use of the Programmable Microwave Tuner System. Finally, the encouragement and support of Dr. B. S. Perlman and Dr. Y. S. Narayan are appreciated.

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In 1962, he joined the Raytheon Microwave and Power Tube Division as a Senior Research and Development Engineer. He participated in microwave tube development and performed experimental and theoretical research on linear-beam and cross-field devices. In 1967, he became Visiting Assistant Professor of Electrical Engineering at the University of Michigan, and in 1969 was appointed Associate Professor. In addition to teaching courses on physical electronics and microwave measurements, he was engaged in sponsored research on microwave semiconductors with emphasis on transferred-electron devices. In 1973, Dr. Curtice joined RCA Laboratories, Princeton, NJ, as a member of the Technical Staff in the Microwave Technology Center. For several years, he directed the development of second-harmonic-extraction TRAPATT amplifiers for *X*-band operation. He has developed two-dimensional computer models of GaAs transferred-electron logic devices and field-effect transistors and computer simulation programs useful in the development of gigabit-rate GaAs and GaInAs integrated circuits. He directed small-signal and large-signal FET modeling programs. In 1984, he received an RCA Laboratories Outstanding Achievement Award for the development of advanced techniques for the computer simulation of III–V-compound FET's. In 1987, he became Manager of GaAs CAD and Modeling for Microwave Semiconductor Corporation in Somerset, NJ.

Dr. Curtice has authored over 40 technical papers and has ten U.S. patents issued to him. He is a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Xi. He was Chairman of IEEE's Boston Section of the Electron Devices group from 1966 to 1967, and Chairman of the Southeastern Michigan Section of the combined MTT, ED, and AP groups for 1972. For 1985–1986, he was Chairman of the combined MTT/ED Chapter at Princeton, NJ. He is presently the treasurer for the Princeton Section of the IEEE.